RESIDUAL STRESS AND FRACTURE OF THICK DIELECTRIC FILMS FOR POWER MEMS APPLICATIONS

X. Zhang, K-S Chen[†], and S. M. Spearing[‡]

Department of Manufacturing Engineering and Fraunhofer USA Center for Manufacturing Innovation,
Boston University, Boston, MA 02215, USA
[†]Department of Mechanical Engineering, National Cheng-Kung University, Tanan, Taiwan 70101
[‡]Department of Aeronautics & Astronautics, Massachusetts Institute of Technology, Cambridge, MA 02139, USA

ABSTRACT

This paper presents residual stress characterization and fracture analysis of thick PECVD oxide films. The motivation for this work is to elucidate the factors contributing to residual stress, deformation and fracture of oxide films so as to refine the microfabrication process for power MEMS manufacturing. The stress-temperature behavior of PECVD oxide films during annealing was studied. Analyses of residual stress relaxation, intrinsic stress generation, and the large deformation response of wafers were carried out. Preliminary experimental observations and estimates of oxide fracture were also provided.

INTRODUCTION

PECVD oxide films are widely used to create both electrical and mechanical elements in MEMS. For power MEMS, thicker oxide layers are often desired in order to obtain higher electrical and mechanical levels [1,2]. However, the ability to deposit oxide film with thickness significantly greater than the current capability of a few micrometers is largely limited by the stress level present in the film.

Residual stress in oxide films leads to large overall wafer bow which makes further processing difficult, such as chemical mechanical polishing or wafer bonding [1,2]. PECVD oxide films are typically compressive, bowing the wafer with the film on the convex surface. Furthermore, thicker films are prone to fracture.

In short, excessive wafer bow and cracking in thick oxide films prohibit process integration within a micro-device, and most importantly, the deleterious effect of residual stress tends to increase with the oxide film thickness. This paper builds on a preliminary work reported previously by us [3].

EXPERIMENTS AND RESULTS

In this study, PECVD oxide films were deposited using a five-station continuous plasma processing system (Concept One[TM], Novellus[TM] Inc.) [4]. Deposition of silane-based oxide films was carried out at 400°C with deposition rates on the order of 1 µm/min. Tetraethylorthosilicate (TEOS)-based oxide was deposited at 350°C; the deposition rate was about 0.25 µm/min.

Oxide films produced by PECVD normally contain significant concentrations of hydrogen. A standard approach to minimizing this problem is to incorporate a high temperature densification process to drive off the hydrogen, so as to achieve dense films. Secondary Ion Mass Spectroscopy (SIMS) analysis was applied to measure hydrogen content in the oxide films. As shown in Figure 1, the hydrogen content in both silane-based oxide and TEOS-based oxide films is in the range of 1-5 at.%, but falls significantly after annealing.
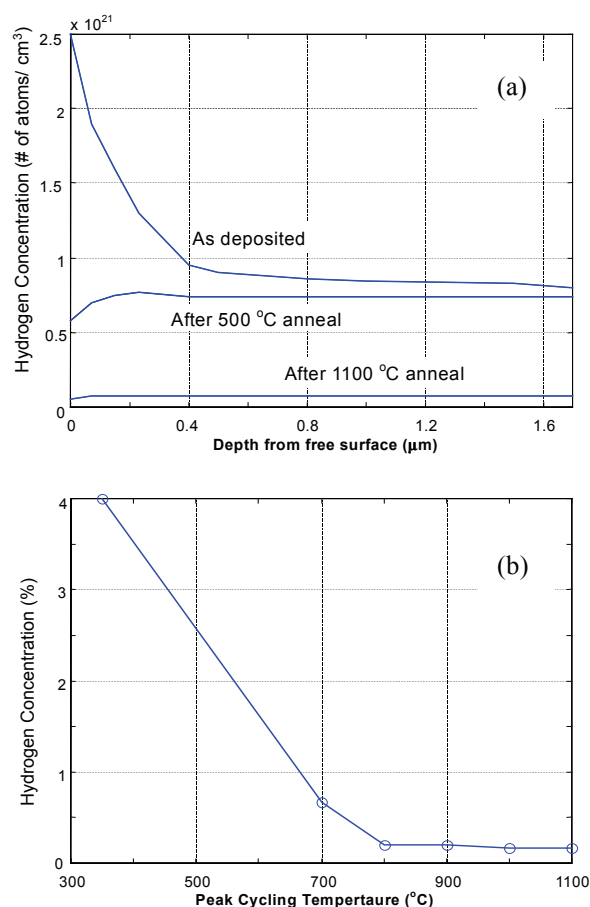

Figure 1: *SIMS hydrogen composition analyses: (a) Silane-based PECVD oxide at as-deposited, after 500°C, and after 1100°C densification, and (b) Hydrogen bulk concentration of TEOS-based PECVD oxide during annealing.*

A better understanding of stress/bow behavior before and after densification process is the first goal of this work. A graph of room temperature wafer bow versus oxide thickness is shown in Figure 2. Figure 2(a) plots results for the silane-based oxide while Figure 2(b) provides data for the TEOS-based oxide. It is seen that in both cases the wafer

bow is proportional to the film thickness and it is much larger for 1100°C densified films than for the as-deposited films.

Thermal cycling tests were conducted in order to assess the role of temperature-dependent effects in determining the state of residual stress in the films. *In situ* wafer curvature was measured between room temperature and 500°C using a KLA-Tencor[TM] FLX-2320 system with a ramp rate of about 5°C/min. Figure 3 shows the residual stress of a silicon wafer coated with 40 μm of silane-based oxide as a function of temperature during thermal cycling to 500°C. The dependence of residual stress on temperature is obviously nonlinear with significant hysteresis during the first thermal cycle.
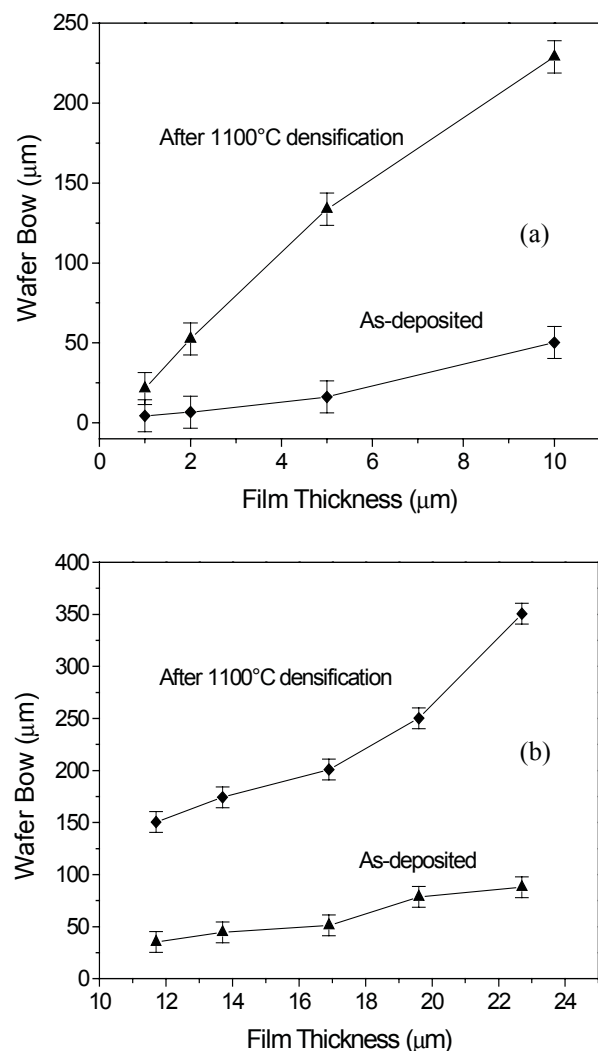

Figure 3: *500°C thermal cycling curves of a 40 μm thick silane-based PECVD oxide film.*

of between 0.5°C/min (near peak temperature) and 10°C/min (below deposition temperature) were used. Stabilization time of 30 mins to 10 hrs were set at the peak temperature to simulate annealing conditions. Observations of defects and curvature were made after each cycle.

As shown in Figure 4(a), cracks spanning the entire wafer were observed in 20 μm silane-based oxide film after exposure to 800°C. Optical microscopy revealed that many additional micro-cracks had initiated near the wafer edge, laser identification numbers and nucleated surface defects (Figure 4(b)-(d)). Fracture mechanics was used to evaluate the behavior of thick oxide films [3]. The critical temperature for oxide fracture as a function of film thickness was predicted. Figure 5 shows cracking temperature predicted for both surface and channeling cracks.

DISCUSSION

The room temperature residual stress as a function of the peak thermal cycling temperature is shown in Figure 6. It is seen that the response can be divided into three distinct zones. For peak annealing temperatures below 400°C, the residual stress in oxide films is relatively independent of the thermal processing. For temperatures between 400°C and 600°C the compressive residual stress in oxide films was found to decrease sharply when the annealing temperature increased. Upon further annealing at temperatures higher than 600°C, however, the compressive residual stress started to increase as the annealing temperature increased.

Clearly, the residual stress in the oxide films strongly depends on the process parameters. The dissolved hydrogen may play an important role in governing intrinsic stress in oxide films; thermal stress, residual gases and micropore annihilation are also three major factors that control the mechanical characteristics of oxide films. Analyses indicated the theoretical predication and test data are highly correlated.

Figure 2: *Wafer bow of PECVD oxide films as a function of thickness before and after densification at 1100°C for 1 hr. (a) Silane-based PECVD oxide, and (b) TEOS-based PECVD oxide.*

In order to investigate the temperature response between 500°C and 1100°C wafers were subjected to subsequent thermal cycling in an Instron[TM] MDS791 furnace with a CU666D temperature controller. Ramp rates
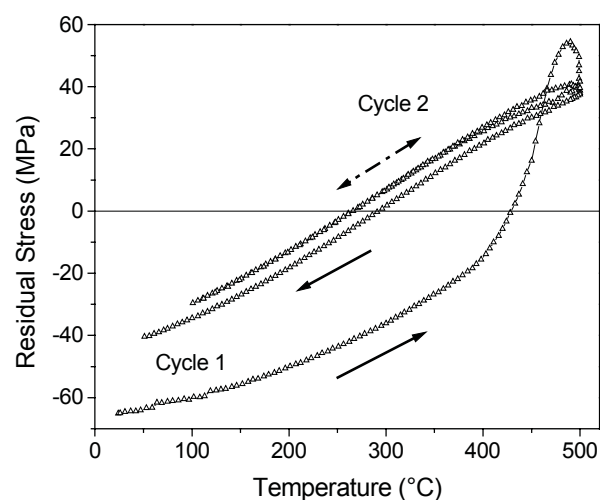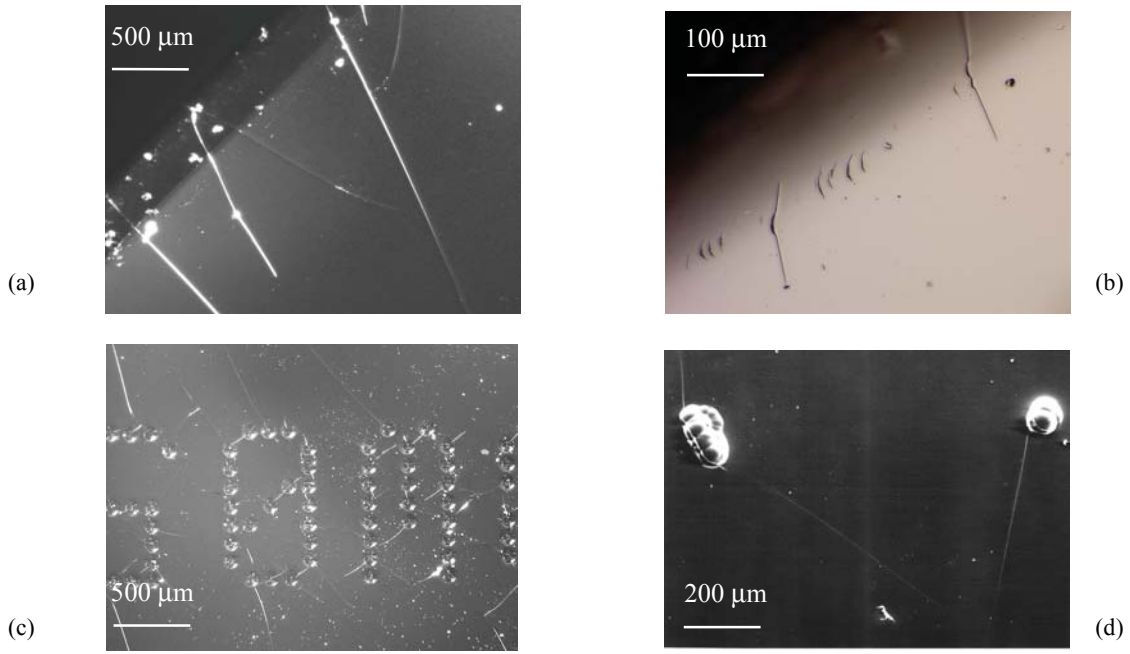
Figure 4: Observations of cracks in thick silane-based oxide films. Cracks were initiated: (a) at the wafer edge in a 20 μm oxide film after thermal cycling at 800°C, (b) at the wafer edge in a 10 μm oxide film after densification at 1100°C for one hour, (c) at the wafer laser ID in a 40 μm oxide film, and (d) at the nucleated surface defects in a 40 μm oxide film.
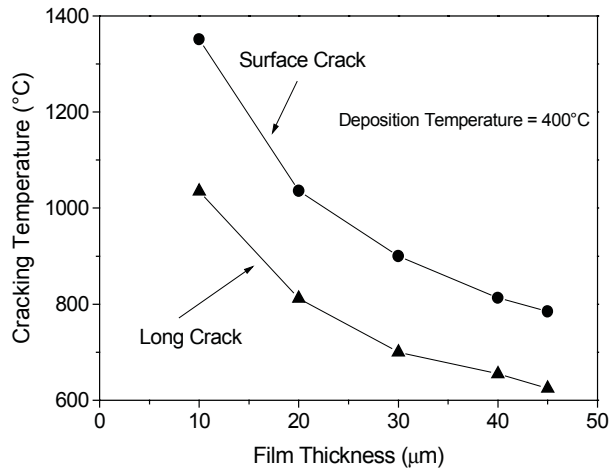

Figure 5: *Cracking temperature predicted by linear elastic fracture mechanics for surface and channeling cracks on silane-based PECVD oxide films.*

Figure 6: *The effect of peak thermal cycling temperature on the room temperature stress of silaned-based PECVD oxide films.*

Based on experiment results, the room temperature residual stress became more compressive as annealing temperature increased; wafer bow in the densified oxide films is much higher than that of the as-deposited films. This is most likely due to thermal stress, as silicon dioxide at high temperatures becomes viscoelastic and stress-free. Hence, residual stress tends to be gradually relieved by material flow, as the temperature increases. As a result, the stress in oxide films becomes more compressive when cooled from a high densification temperature to room temperature. An indication of the magnification of this effect can be obtained by modeling the oxide as a Maxwell fluid. The viscoelastic behavior of oxide materials is shown
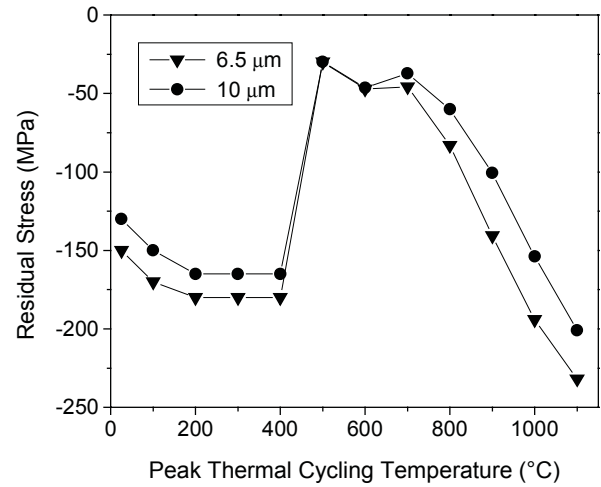
in Figure 7. It is seen that the residual stress is reduced from 74 MPa to about 50 MPa asymptotically, and the relaxation time constant is estimated to be 2500 seconds.

There are many mechanisms that may be responsible for the generation of intrinsic stress in oxide films. Typical models include recrystallization, chemical reactions, incorporation of atoms, dislocation rearrangements, lattice mismatch, excess vacancy annihilation, grain boundary relaxation, and phase transformation etc. A comprehensive summary has been provided by Nix and Doerner *et al.* [5-7]. However, since oxide is an amorphous material, any theory based on the generally used grain-boundary relaxation models are not applicable. In this study, using analytical
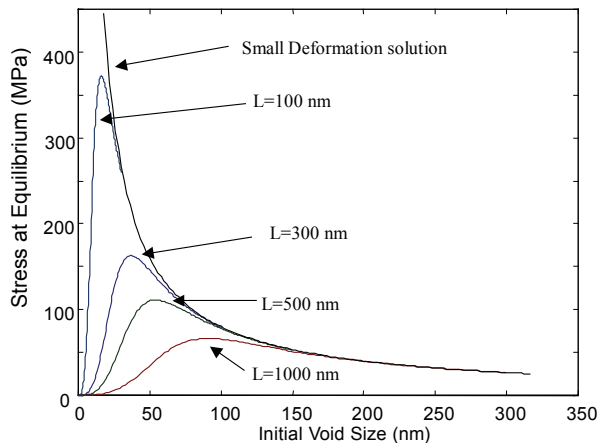
Figure 7: *Estimation of intrinsic stresses generated during void shrinking process for various characteristic length of unit cell.*
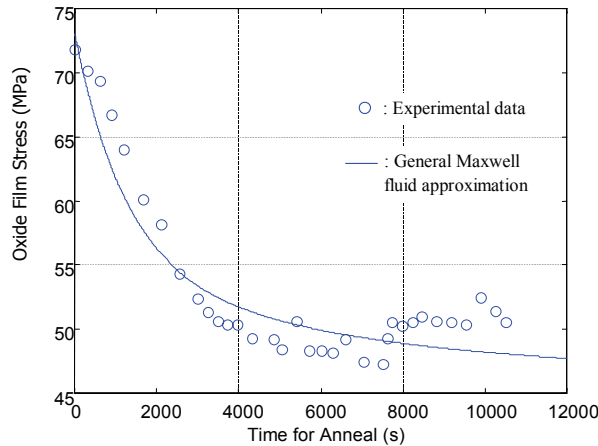

Figure 8: *The experimental data and FEM simulation for stress relaxation during a 500 ℃ annealing.*
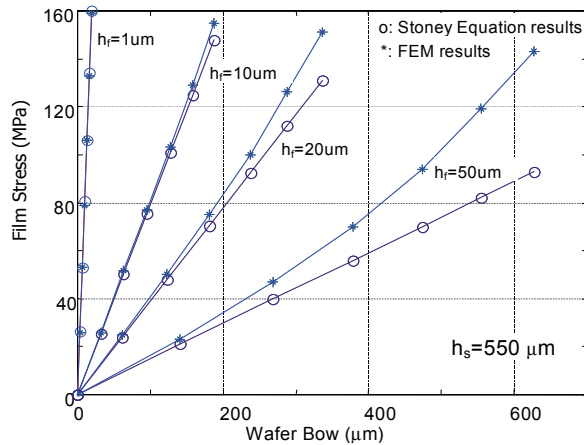

Figure 9: *The relationship between film stress and wafer bow for various oxide film thickness, calculated by Stoney equation or FEM simulation.*

potential energy minimization methods, intrinsic stresses generated during the shrinking of micro-voids was estimated. One of results is shown in Figure 8.

In addition, one further point needs to be pointed out: for a thin film on a silicon substrate, the stress in the film can be calculated by the Stoney equation [8], however, for the case of a relatively thick film on a silicon substrate, the effect of nonlinearlity is significant and must be taken into account. In this work, based on the linear Stoney equation and the nonlinear finite element method (FEM) model, the relationship between film stress and wafer bow for various oxide film thickness was calculated. An example is given in Figure 9. Clearly, the effect of nonlinearlity is increased with increasing oxide film thickness.

CONCLUING REMARKS

This paper provides preliminary results of characterization of PECVD thick oxide films and studies of the stress-temperature behavior during deposition and post-annealing. The ultimate goal is to identify the factors and mechanisms that may contribute to the residual stress and fracture of thick oxide films. Preliminary analysis of theoretical models and methodology for better understanding of hydrogen diffusion, large deformation of wafers, intrinsic stress generation during deposition, stress relaxation at high-temperature annealing, and oxide film fracture during thermal processing were provided. Future work would be emphasized on the investigation of appropriate engineering solutions and process innovations for PECVD thick oxide deposition that can effectively reduce wafer distortion as well as prevent film failure.

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